IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. (Currently Amended) A data processing apparatus that arbitrates sharing of a single semiconductor memory circuit among multiple data processing circuits, comprising:

a semiconductor memory circuit that executes operations corresponding to a command signal, address signal and clock signal received external to the semiconductor memory circuit; and

a data processing circuit that supplies the semiconductor memory circuit with a clock enable signal for enabling an input of the clock signal when active and a disabling the input of the clock signal when inactive, and a chip select signal for enabling input of command signals when the chip select signal is active and disabling input of command signals when the chip select signal is inactive; wherein

before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the clock enable signal and chip select signal, a different data processing circuit starting control of the semiconductor memory circuit supplies a clock enable signal and chip select signal values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit.

2. (Original) The data processing apparatus of claim 1, wherein:

the data processing circuit supplies a sharing arbitration circuit with a request when requesting control of the semiconductor memory circuit, controls the semiconductor memory circuit in response to a grant signal, and supplies the arbitration circuit with a busy signal while controlling the semiconductor memory circuit;

when ending control of the semiconductor memory circuit, the data processing circuit stops supplying the clock enable signal and chip select signal a predetermined time after stopping the supply of the busy signal; and

the sharing arbitration circuit generates the grant signal in response the request signal before the predetermined time has elapsed.

3. (Original) The data processing apparatus of claim 1, wherein:

the semiconductor memory circuit enters a lower power state when the clock enable signal is inactive, as compared to when the clock enable signal is active.

4. (Original) The data processing apparatus of claim 1, wherein:

one of the multiple data processing circuits is a master device while any others are slave devices; and

the master device supplies the clock enable signal and chip select signal to the semiconductor memory circuit when none of the slave devices provides the clock enable signal and chip select signal to the semiconductor memory circuit.

5. (Original) The data processing apparatus of claim 1, wherein:

the multiple data processing circuits are connected to one another but formed independently of one another.

6. (Original) The data processing apparatus of claim 2, wherein:

one of the multiple data processing circuits is a master device while any others are slave devices; and

the sharing arbitration circuit is built into the master device.

7. (Original) The data processing apparatus of claim 1, wherein:

each of the data processing circuits of the multiple data processing circuits includes a built in sharing arbitration circuit;

the multiple data processing circuits are initialized to establish one data processing circuit as a master device and all others as slave devices; and

the arbitration circuit of the master device is enabled and the arbitration circuits of the slave devices are disabled.

8. (Original) The data processing apparatus of claim 7, wherein:

in an initialization operation, the sharing arbitration circuit built into the master device supplies at least one slave device with a grant signal; and

the at least one slave device supplies a request signal of a predetermined time period if the grant signal is received while the slave device is not supplying its own request signal; wherein

the sharing arbitration circuit built into the master device stops supplying the grant signal once the startup of the at least one slave device is confirmed by input of the request signal from the at least one slave device.

9. **(Currently Amended)** A data processing apparatus, comprising:

a semiconductor memory circuit that is controlled by **control signal** inputs to at least one control input;

at least one control line coupled to the **at least one** control input of the semiconductor memory circuit; and

a plurality of data processing circuits that share access to the semiconductor memory circuit, each **data processing circuit** having a control output coupled to the **at least one** control line; wherein

when one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal; and

subsequently, when ~~one~~ **another** data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

10. (Original) The data processing apparatus of claim 9, wherein:

the semiconductor memory circuit operates in synchronism with a clock signal, and the at least one control input includes

a chip select input that enables the processing of commands by the semiconductor memory circuit, and

a clock enable signal that enables generation of timing signals within the semiconductor memory circuit.